



Docket No.: MAS-FIN-153

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German Application No. 101 10 203.8, filed March 2, 2001.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Hollywood, Florida

---

Christine Kahl

October 1, 2003

Lerner & Greenberg, P.A.  
P.O. 2480  
Hollywood, FL 33022-2480  
Tel.: (954) 925-1100  
Fax.: (954) 925-1101



## Description

Electronic component with stacked semiconductor chips

The invention relates to an electronic component with stacked semiconductor chips and to a method for its production according to the independent claims.

For more compact stacking or higher integration of electronic components, and in particular integrated semiconductor components, known as semiconductor chips, they can be stacked in a number of layers. In this case, both individual semiconductor chips and larger units made up of semiconductor chips can be stacked before they are separated, i.e. as semiconductor wafers, as they are known. To interconnect the semiconductor chips or wafers arranged one on top of the other electrically and mechanically at their contacts, they are soldered. For this purpose, apertures can be etched into the wafer by means of an etching process. The inner surfaces of these apertures are subsequently metallized. In this way, a number of wafers can be mechanically and electrically connected by means of a soldered joint, and in this way stacked one on top of the other.

For producing stacked three-dimensional topographies of semiconductor chips, known as chip-size packages (CSP), wafers are divided along separating joins between the individual semiconductor chips by means of an etching process, in order after that to establish wiring links from the respective active sides of the semiconductor chips to their rear sides with the contact connections and bonding areas to be soldered that are located on these sides.

The object of the invention is to provide an electronic component with stacked semiconductor chips which has stable mechanical and electrical connections between the semiconductor chips to be stacked, along with a minimal spatial extent.

This object is achieved by the subject-matter of the independent claims. Features of advantageous developments of the invention emerge from the subclaims.

According to the invention, the electronic component has at least two stacked semiconductor chips, which are respectively mounted on a wiring board and electrically connected to the latter. The at least two wiring boards are stacked one on top of the other essentially parallel to one another and interconnected mechanically and electrically by means of soldered connections. The soldered connections extend through apertures in at least one of the wiring boards and over one or more levels of wiring boards stacked one on top of the other, with semiconductor chips mounted on these boards.

The electronic component according to the invention has the advantage that three-dimensionally structured components can be produced from stacked semiconductor chips in a simple and exact way. These components can be made very compact and have great mechanical stability.

In one embodiment of the invention, the soldered connections are provided in edge regions of the at least two stacked wiring boards. This embodiment has the advantage that the soldered connections act as load-bearing mechanical connections and at the same time can provide the electrical connection of the semiconductor chips to one another.

A further embodiment provides that the soldered connections are respectively formed by solder balls lying one on top of the other and fused together. In this embodiment, it is of advantage that an exactly defined position of the wiring boards with the semiconductor chips mounted on them is made possible in an easy way in terms of production engineering. The subsequently fused together solder balls provide an electrically and mechanically good connection.

In a further embodiment of the invention, it is provided that the solder balls to be fused have a smaller diameter than the apertures in the wiring boards. This embodiment has the advantage that, by simply putting solder balls in place, wiring boards can be stacked one on top of the other and the solder balls fused while maintaining the distance predetermined by a plastic buffer, such as for example a bonding channel covering.

A further embodiment according to the invention provides that the at least two wiring boards with the semiconductor chips mounted on them are stacked one on top of the other in such a way that a rear side of one semiconductor chip is facing an underside of a neighboring wiring board. This embodiment has the advantage that minimal distances between the individual stacking levels can be realized in this way.

A further embodiment of the invention provides that the undersides of the wiring boards are provided with supporting points, on which a rear side of a semiconductor chip respectively comes to bear. What is especially advantageous about this embodiment is that the supporting points represent a defined bearing point for the successively following wiring boards of the stack. Even if there are slight differences in

the diameter of the solder balls and/or of the apertures in which they come to lie, there is no risk of any direct contact between the wiring board and the semiconductor chip of different stacking levels.

In a further embodiment according to the invention, the supporting points take the form of plastic buffers arranged centrally on the rear sides of the wiring boards, which has the advantage of an insulating effect in mechanical, electrical and thermal respects.

In a further embodiment according to the invention, the plastic buffers consist of an elastomer, which has in particular the advantage of effective mechanical damping between the surfaces in contact with them.

A further embodiment of the invention provides that an uppermost and/or undermost wiring board of a stack is provided with near-edge electrical contacts without apertures. This embodiment has the advantage that the liquefied solder of the fused solder ball is kept on the contact area and cannot flow away toward a side on which no further wiring board is attached.

A further embodiment of the invention provides that an undermost wiring board of a stack is provided with contact terminal areas, accompanied by the advantage that this wiring board can be directly bonded with further electric circuits.

A further embodiment of the invention provides that an undermost wiring board of a stack is provided with contact bumps, accompanied by the advantage that this wiring board can be directly mounted and electrically bonded on a printed circuit board or the like.

A further embodiment of the invention provides that an undermost wiring board of a stack is provided with solder deposits located on the contact terminal areas. This embodiment has the advantage that the undermost wiring board can be connected to further electric circuits in a simple way by melting these solder deposits.

A further embodiment of the invention provides that the wiring boards which are not the undermost or uppermost of a stack are provided with near-edge electrical contacts with apertures, which has the advantage that the solder balls coming to bear in the apertures provide an exact distance of the wiring boards from one another in the stacked state. In the molten state, the apertures provide the special advantage of a soldered connection that extends over a number of levels of the stack and is consequently mechanically very stable.

A further embodiment of the invention provides that the wiring boards which are not the undermost or uppermost of a stack are provided with near-edge electrical contacts without apertures. This is accompanied by the advantage of different electrical bonding of the contact points from both sides, since no plating through takes place.

In a method for producing an electronic component which has at least two stacked semiconductor chips which are respectively mounted on a wiring board and electrically connected to the latter, it is provided that the at least two wiring boards are stacked one on top of the other essentially parallel to one another and interconnected mechanically and electrically by means of soldered connections. Moreover, the soldered connections extend through apertures in at least one of the wiring boards and over one or more levels of wiring boards

stacked one on top of the other with semiconductor chips mounted on them. According to the invention, the method comprises the following method steps. After preparing wiring boards with semiconductor chips mounted on them and electrically connected to them, supporting points are applied to the rear sides of the wiring boards facing away from the semiconductor chips. After that, solder is provided in near-edge apertures of the wiring boards, with electrical contacts adjoining the apertures. Parallel stacking of at least two wiring boards with semiconductor chips mounted on them subsequently takes place, a passive rear side of a semiconductor chip respectively coming to bear on a supporting point. Finally, the solder is melted, whereby mechanical and electrical connections are established between the adjoining levels of the stack.

This method has the advantage that very compact and highly integrated electronic components with semiconductor chips can be produced in this way. Moreover, the method has the advantage that a high level of precision is obtained in production, i.e. the geometrical dimensions and positions of the parts to be connected to one another can be maintained very exactly with the method according to the invention. With the aid of the method according to the invention, the stacking of a large number of individual assemblies comprising wiring boards and semiconductor chips mounted on them is possible.

In a first exemplary embodiment of the method, the solder is provided in the apertures in the form of solder balls which have a smaller diameter than the apertures. This exemplary embodiment has the advantage of an optimally defined position of the stacked wiring boards in relation to one another. On the basis of the predetermined geometrical dimensions of the apertures, solder balls and the distance between the wiring

boards stacked one on top of the other, they can be fixed and connected approximately in parallel and at a defined distance in relation to one another with minimal tolerance.

In a further exemplary embodiment of the method, the solder is provided in the apertures in the form of solder paste. This further exemplary embodiment has the advantage that the solder paste adheres very well on the metallic contact terminal areas, even under unfavorable conditions, allowing the risk of a defectively soldered connecting point to be minimized.

For a further exemplary embodiment of the method, it is provided that the wiring boards are mechanically fixed during the stacking and before the soldering, which has the advantage of a very low defect or reject rate in the production of the stacked electronic components. Moreover, in this way, handling of the individual parts to be processed and connected is also possible in any desired position.

An alternative example of how the method is carried out provides that firstly a number of semiconductor wafers are stacked one on top of the other and, after connecting the contact vias with the conductor tracks of semiconductor wafers lying above or below, the stacked semiconductor wafers are individually separated into stacked semiconductor chips.

This example of how the method is carried out has the advantage that a very efficient way of processing relatively large batches is made possible. The forming of stacked assemblies on the wafer level can make it possible for the production equipment to achieve a higher throughput.

A further exemplary embodiment of the method according to the invention provides that, for melting the soldered joints for

connecting the stacked wiring boards, the latter are heated to a soldering temperature, which has the advantage of a very quick and reliable connection, and consequently very quick and efficient processability.

To sum up, the following aspects of the invention are obtained. The electronic component according to the invention may comprise a number of stacked assemblies which are respectively formed by a wiring board, known as the substrate carrier (also referred to as an interposer), and a semiconductor chip fastened on it with positive engagement. The wiring of the contact terminals of the semiconductor chip, some of which are microscopic, to form larger contact terminal areas suitable for further processing takes place on the wiring board. This mentioned assembly is also referred to as a CSP (chip-size package). Provided at the edge of the wiring board are contact terminal areas, known as landing pads, on which solder balls are provided; in a subsequent production step, the solder balls are melted and provide an electrical and mechanical connection to further wiring boards, or else for mounting on a printed circuit board or the like.

The individual assemblies - comprising wiring boards and semiconductor chips - are interconnected both mechanically and electrically by means of the solder balls. What is important here is that the respective connecting points are arranged vertically one above the other and that the respective contact terminal area (landing pad) has a sufficiently large opening, so that a solder ball placed on top of it can contact a solder ball lying under it. During the soldering, known as the reflow process, the solder balls become molten and fuse together. Once the solder has solidified, connections of one wiring board to the respectively adjoining wiring board consequently form. As an option instead of the solder balls

described, it is also possible to use solder paste, which is applied to the respective connecting point by means of what is known as a dispensing device. In this case, no openings or apertures are required in the contact terminal areas at the outer edge of the wiring boards.

The invention is explained in more detail below on the basis of embodiments with reference to the attached figures.

Figure 1 shows a schematic cross section of a wiring board with a semiconductor chip mounted on it, before stacking.

Figure 2 shows two wiring boards stacked one on top of the other, corresponding to figure 1.

Figure 3 shows two wiring boards stacked one on top of the other and securely connected to each other in a schematic cross section.

Figure 4 shows two wiring boards stacked one on top of the other, corresponding to figure 3, with solder balls having been provided on an uppermost wiring board.

In the following descriptions of figures, exemplary embodiments of the invention are represented. The same parts are always provided with the same reference numerals in the figures and in some cases are not explained more than once.

Figure 1 shows a schematic cross section of a wiring board 5 with a semiconductor chip 2 mounted on it, before stacking with further wiring boards. The semiconductor chip 2 is mounted with its active front side 3, which has semiconductor structures, on the flat wiring board 5 with positive engagement. On the flat side of the wiring board 5 facing

away from the semiconductor chip 2 there can be seen a plastic buffer 14, which is explained below with reference to figure 2.

At the outer edge of the wiring board 5, it is provided with contacts 6, which are connected to conductor tracks (not shown here). The conductor tracks lead to contacts, which have electrical connections with contact terminal areas of the semiconductor chip 2. Respectively provided on the metallic contacts 6 are solder balls 10, which, after the stacking of two or more wiring boards 5, are melted and provide an electrical and mechanical connection of the wiring boards.

Figure 2 shows a schematic cross section of two wiring boards 5 stacked one on top of the other. The plastic buffer 14 fastened centrally on each wiring board 5 is in this case in contact with the passive rear side 4 of the semiconductor chip 2 mounted on the next wiring board 5. The wiring board 5 that is undermost in the figure represented is provided at its outer edge with electrical contacts 6 without apertures, on which solder balls 10 respectively rest. The further wiring board 5 resting on this undermost wiring board is likewise provided at its outer edge with electrical contacts 6, which respectively have an aperture 8. In this case, the electrical contacts 6 of the wiring boards 5 lying one on top of the other lie approximately congruently one above the other, so that the solder balls 10 located in the apertures 8 come to lie vertically one above the other.

Figure 3 shows a schematic cross section of two wiring boards 5 stacked one on top of the other and securely interconnected. In this case, the solder balls 10 respectively lying one above the other are melted by heating and in each case form a soldered connection 12 extending through the entire stack.

Each soldered connection 12 provides a mechanical fixing of the stacked wiring boards 5 and at the same time represents an electrical connection between the electrical contacts 6 lying one above the other.

Figure 4 shows a further schematic cross section of two wiring boards 5 stacked one on top of the other and securely interconnected. On an uppermost wiring board 5, solder balls 10, which can provide a secure mechanical and electrical connection on a mounting location by means of melting, are in this case respectively provided on contact terminal areas - not shown here.

The contacts 6 at the edge of the wiring boards 5 may either be provided along all the edges of each wiring board or, if appropriate, be located only on two oppositely lying sides of the wiring boards.

An exemplary embodiment of the production method according to the invention for producing an electronic component is described below on the basis of figures 1 to 4 explained above.

Firstly, semiconductor chips 2 with passive rear sides 4 without integrated circuits and with active front sides 3 with integrated circuits are prepared. These semiconductor chips 2 are in each case mechanically and electrically connected with positive engagement to wiring boards 5, which respectively have electrical contacts 6 on at least two oppositely lying side edges. On the surfaces of the wiring boards 5 facing away from the semiconductor chips 2, supporting points are respectively applied in an approximately central position in the form of plastic buffers 14.

Apart from those of the undermost wiring board, the contacts 6 of the wiring boards 5 are respectively provided with apertures 8, into which solder balls 10 are placed. This is followed by at least two wiring boards 5 being stacked in parallel, so that their contacts 6 come to lie with the apertures 8 located in them and the solder balls 10 placed in the apertures 8 one above the other. The passive rear sides 4 of the semiconductor chips 2 in this case come to bear respectively on a plastic buffer 14 of an adjoining wiring board 5. By heating the stack, the solder balls 10 are fused to form continuous soldered connections 12, which provide a mechanical connection of the stack and an electrical connection of the contacts 6 to one another.

The electronic component according to the invention may be formed by a multiplicity of semiconductor chips mounted on wiring boards and stacked one on top of the other. The stacked wiring boards do not necessarily have to be of the same dimensions. All that is important is that, when there are two wiring boards lying one on top of the other, at least two or more contacts with apertures and solder balls placed in them come to lie congruently one above the other. The soldered connections extending over the stack do not have to be continuous soldered connections from the lowermost to the uppermost wiring board. Similarly possible are soldered connections which are continuous over certain sections, which in each case connect two or more wiring boards. In this way, electronic components can be formed from any desired stacks of wiring boards of different sizes with semiconductor chips of different sizes mounted on them.

## Patent claims

1. An electronic component with at least two stacked semiconductor chips (2), which are respectively mounted on a wiring board (5) and electrically connected to the latter, the at least two wiring boards (5) being stacked one on top of the other essentially parallel to one another and interconnected mechanically and electrically by means of soldered connections (12), the soldered connections (12) extending through apertures (8) in at least one of the wiring boards (5) and over one or more levels of wiring boards (5) stacked one on top of the other, with semiconductor chips (2) mounted on these boards.
2. The electronic component as claimed in claim 1, characterized in that the soldered connections (12) are provided in edge regions of the at least two stacked wiring boards (5).
3. The electronic component as claimed in claim 1 or 2, characterized in that the soldered connections (12) are respectively formed by solder balls (10) lying one on top of the other and fused together.
4. The electronic component as claimed in one of claims 1 to 3, characterized in that the solder balls (10) to be fused have a smaller diameter than the apertures (8) in the wiring boards (5).
5. The electronic component as claimed in one of the preceding claims, characterized in that the at least two wiring boards (5) with the semiconductor chips (2) mounted on them are stacked one on top of the other in such a way that a

rear side (4) of one semiconductor chip (2) is facing an underside of a neighboring wiring board (5).

6. The electronic component as claimed in one of the preceding claims, characterized in that the undersides of the wiring boards (5) are provided with supporting points, on which a rear side (4) of a semiconductor chip (2) respectively comes to bear.

7. The electronic component as claimed in claim 6, characterized in that the supporting points take the form of plastic buffers (14) arranged centrally on the rear sides of the wiring boards (5).

8. The electronic component as claimed in claim 7, characterized in that the plastic buffers (14) consist of an elastomer.

9. The electronic component as claimed in one of the preceding claims, characterized in that an uppermost and/or undermost wiring board (5) of a stack is provided with near-edge electrical contacts (6) without apertures (8).

10. The electronic component as claimed in one of the preceding claims, characterized in that an undermost wiring board (5) of a stack is provided with contact terminal areas (16).

11. The electronic component as claimed in one of the preceding claims, characterized in that an undermost wiring board (5) of a stack is provided with contact bumps.

12. The electronic component as claimed in one of the preceding claims, characterized in that an undermost wiring

board (5) of a stack is provided with solder deposits located on the contact terminal areas (16).

13. The electronic component as claimed in one of the preceding claims, characterized in that the wiring boards (5) which are not the undermost or uppermost of a stack are provided with near-edge electrical contacts (6) with apertures (8).

14. The electronic component as claimed in one of the preceding claims, characterized in that the wiring boards (5) which are not the undermost or uppermost of a stack are provided with near-edge electrical contacts (6) without apertures (8).

15. A method for producing an electronic component which has at least two stacked semiconductor chips (2) which are respectively mounted on a wiring board (5) and electrically connected to the latter, the at least two wiring boards (5) being stacked one on top of the other essentially parallel to one another and interconnected mechanically and electrically by means of soldered connections (12) and the soldered connections (12) extending through apertures (8) in at least one of the wiring boards (5) and over one or more levels of wiring boards (5) stacked one on top of the other with semiconductor chips (2) mounted on them, the method having the following method steps:

- preparing wiring boards (5) with semiconductor chips (2) mounted on them and electrically connected to them,
- applying supporting points to the rear sides of the wiring boards (5) facing away from the semiconductor chips (2),
- providing solder in near-edge apertures (8) of the wiring boards (5), with electrical contacts (6) adjoining the apertures (8),

- parallel stacking of at least two wiring boards (5) with semiconductor chips (2) mounted on them, a rear side (4) of a semiconductor chip (2) respectively coming to bear on a supporting point,
- melting of the solder, whereby mechanical and electrical connections are established between the adjoining levels of the stack.

16. The method as claimed in claim 15, characterized in that the solder is provided in the apertures (8) in the form of solder balls (10) which have a smaller diameter than the apertures (8).

17. The method as claimed in claim 15, characterized in that the solder is provided in the apertures (8) in the form of solder paste.

18. The method as claimed in one of claims 15 to 17, characterized in that the wiring boards (5) are mechanically fixed during the stacking and before the soldering.

19. The method as claimed in one of claims 15 to 18, characterized in that firstly a number of semiconductor wafers are stacked one on top of the other and, after connecting the contact vias with the conductor tracks of semiconductor wafers lying above or below, the stacked semiconductor wafers are individually separated into stacked semiconductor chips (2).

20. The method as claimed in one of claims 15 to 19, characterized in that, for melting the soldered joints for connecting the stacked wiring boards (5), the latter are heated to a soldering temperature.

21. The method as claimed in one of claims 15 to 20 for producing an electronic component as claimed in at least one of claims 1 to 14.

## Abstract

### Electronic component and method for its production

The invention relates to an electronic component with at least two stacked semiconductor chips (2), which are respectively mounted on a wiring board (5). The wiring boards are stacked one on top of the other and interconnected mechanically and electrically by means of soldered connections (12). The soldered connections extend through apertures (8) in the wiring boards and over one or more levels of wiring boards stacked one on top of the other, with semiconductor chips mounted on these boards. The invention also relates to a method for producing the electronic component.

[Figure 4]

List of designations

- 2 semiconductor chip
- 3 active front side
- 4 passive rear side
- 5 wiring board
- 6 contact
- 8 aperture
- 10 solder ball
- 12 soldered connection
- 14 plastic buffer
- 16 contact terminal area